Claims

What is claimed as new and desired to be protected by Letter Patent of the United States is:

1. A demodulator for phase modulated (PM) signals comprising:
   A direct phase sampler / digitizer;
   A differencing circuit;
   A "p" deep running averager;
   A digital subtractor;
   A phase to amplitude converter.
2. A demodulator as in claim 1, wherein the direct phase digitizer provides the instantaneous phase of the input signal, at the time of the clock transitions.
3. A demodulator as in claim 1, wherein a differencing circuit generates on every clock cycle the phase difference in the input signal over the clock period.
4. A demodulator as in claim 1, wherein a running averager generates a running average of phase differences over the last "p" consecutive phase differences.
5. A demodulator as in claim 1, wherein a subtractor subtracts the average phase difference generated by the averager from the instantaneous phase difference calculated by the differencing circuit and generates a digital data which indicates the instantaneous phase deviation.
6. A demodulator as in claim 1, wherein a phase to amplitude converter converts the instantaneous phase deviation generated by the subtractor into an amplitude directly proportional to the phase deviation.
7. A running averager as in claim 4, wherein "p" the depth of the averaging span determines the precision for the center frequency.
8. A phase to amplitude converter as in claim 6, wherein the conversion of phase information into a voltage output is obtained by a sine lookup table followed by a digital to analog converter.
9. A phase to amplitude converter as in claim 6, wherein the conversion of phase information into a voltage output is obtained by converting binary code presentation of the phase information into a Grey code followed by further processing using EXOR functions, bit drivers and a resistive network.

~~10.~~ DELETAD ~~A demodulator for frequency modulated (FM) signals comprising:~~
~~A direct phase sampler / digitizer;~~
~~A differencing circuit;~~
~~A "p" deep running averager;~~
~~A second "q" deep running averager~~

~~A digital subtractor;~~

~~A phase to amplitude converter.~~

~~11.~~ DELETAD ~~A demodulator as in claim 10, wherein the direct phase digitizer provides the instantaneous phase of the input signal, at the time of the clock transitions.~~

~~12.~~ DELETAD ~~A demodulator as in claim 10, wherein a differencing circuit generates on every clock cycle the phase difference in the input signal over the clock period.~~

~~13.~~ DELETAD ~~A demodulator as in claim 10, wherein a running averager generates a running average of phase differences over the last "p" consecutive phase differences.~~

~~14.~~ DELETAD ~~A demodulator as in claim 10, wherein a second running averager generates a running average of phase differences over the last "q" consecutive phase differences.~~

~~15.~~ DELETAD ~~A demodulator as in claim 10, wherein a subtractor subtracts the average phase difference generated by the averager from the instantaneous phase difference calculated by the differencing circuit and generates a digital data which indicates the instantaneous phase deviation.~~

~~16.~~ DELETAD ~~A demodulator as in claim 10, wherein a phase to amplitude converter converts the instantaneous phase deviation generated by the subtractor into an amplitude directly proportional to the phase deviation.~~

~~17.~~ DELETAD ~~A running averager as in claim 13, wherein "p" the depth of the averaging span determines the precision for the center frequency.~~

~~18.~~ DELETAD ~~A second running averager as in claim 14, wherein "q" the depth of the averaging span of the second averager determines the bandwidth of the demodulated signal output.~~

~~19.~~ DELETAD ~~A phase to amplitude converter as in claim 16, wherein the conversion of phase information into a voltage output is obtained by a sine lookup table followed by a digital to analog converter.~~

~~20.~~20. A phase to amplitude converter as in claim 6, wherein the conversion of phase information into a voltage output is obtained by converting binary code presentation of the phase information into a Grey code followed by further processing using EXOR functions, bit drivers and a resistive network.

~~21.~~ DELETAD ~~An FM or PM receiver comprising:~~

~~A quadrature input signal generator;~~

~~A direct digital phase digitizer;~~

~~A digital demodulator.~~

~~22.~~ DELETAD ~~A receiver as in claim 21, wherein the quadrature generation may be obtained by quadrature down conversion or by any type of quadrature power splitter.~~

~~23.~~ b DELETAD ~~A demodulator as in claim 21, wherein the direct phase digitizer provides the instantaneous phase of the input signal, at the time of the clock transitions.~~

~~24.~~ DELETAD ~~A receiver as is claim 21, wherein the demodulator contains no tuned or resonant circuits and wherein the operation of the demodulator is controlled by a clock.~~

~~25.~~ DELETAD ~~A converter to convert binary code presentation of the phase of a signal into a magnitude of voltage or current comprising:~~

~~EXOR Logic to convert the binary code into Grey code;~~

~~EXOR logic to generate specific driver code;~~

~~A resistive network to convert the drive code into a voltage or current.~~

~~26.~~ DELETAD ~~A converter as in claim 25, wherein the conversion of binary code to Grey code is obtained using the formula~~ $\cancel{G_n = B_n \oplus B_{n+1}}$~~, and wherein~~ $\cancel{G_n}$ ~~represents a Grey code bit n and~~ $\cancel{B_n}$ ~~represents a binary code bit n.~~

~~27.~~ DELETAD ~~A converter as in claim 25, wherein the drive code is obtained from the Grey code using the formula~~ $\cancel{D_k|_0^n = G_k \oplus G_{k+1} \oplus G_{k+2} \oplus ... \oplus G_n}$~~, and wherein~~ $\cancel{D_k}$ ~~represents a drive bit k.~~

28. (NEW) A digital demodulator for phase modulated (PM) signals wherein a digital input is a digital presentation of the instantaneous phase of the modulated signal.

29. (NEW) A demodulator for phase modulated (PM) signals as in claim 11 comprising:

A differencing circuit;

A "p" deep running averager;

A digital subtractor;

A phase to amplitude converter.

30. (NEW) A demodulator as in claim 29, wherein a differencing circuit generates on every clock cycle the phase difference in the input signal over the clock period.

31. (NEW) A demodulator as in claim 29, wherein a running averager generates a running average of phase differences over the last "p" consecutive phase differences.

32. (NEW) A demodulator as in claim 29, wherein a subtractor subtracts the average phase difference generated by the averager from the instantaneous phase difference calculated by the differencing circuit and generates a digital data which indicates the instantaneous phase deviation.

33. (NEW) A demodulator as in claim 29, wherein a phase to amplitude converter converts the instantaneous phase deviation generated by the subtractor into an amplitude directly proportional to the phase deviation.

34. (NEW) A running averager as in claim 31, wherein "p" the depth of the averaging span determines the precision for the center frequency.

35. (NEW) A phase to amplitude converter as in claim 33, wherein the conversion of phase information into a voltage output is obtained by a sine lookup table followed by a digital to analog converter.
36. (NEW) A phase to amplitude converter as in claim 33, wherein the conversion of phase information into a voltage output is obtained by converting binary code presentation of the phase information into a Grey code followed by further processing using EXOR functions, bit drivers and a resistive network.